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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 09/894,203
Filing Date: June 28, 2001
Appellant(s): TOMOHIRO, ICHIRO

Adam Keser, Reg. No. 54,217
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 8/8/2007 appealing from the Office action mailed 10/24/2006.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

No amendment after final has been filed.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is substantially correct.

Claims 1-10 are rejected under 35 U.S.C. 102(b) as being anticipated by Vicard (US Patent 5,708,715).

There is an additional ground of rejection for claims 1-10 as follows:

Claims 1-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vicard, and further in view of Chuang et al. (US Patent 6,031,757, hereinafter Chuang).

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

5,708,715	VICARD	01-1998
6,031,757	CHUANG et al.	02-2000

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claims 1-10 are rejected under 35 U.S.C. 102(b) as being anticipated by Vicard.

Regarding claim 1, Vicard teaches

- at least one non-volatile memory cell array block which is capable of receiving concurrent electrical erasure **(column 2, lines 30-67, column 5, lines 49-67, functional block)**;
- a key means comprising a security release key **(column 4, lines 20-67, col. 5, lines 25-40, chip-key signature)**;
- a lock means comprising a security registration lock corresponding to each of the at least one memory cell array block **(column 4, lines 20-67, lock circuitry)**;
- at least one memory region, each one of said at least one memory region being provided in the at least one memory cell array block, for storing the security release key **(column 5, lines 1-48, signature stored, col. 5, lines 48-67, signatures H(k1)-H(K6) associated w/ particular blocks)**;

- at least one non-volatile storage means for storing the security registration lock **(col. 2, lines 52-67, column 5, lines 48-67, column 6, lines 1-36, lock circuitry)**;
- a determination circuit for comparing a value which is generated based on the security release key **(a signature of the key)** against a value which is generated based on the security registration lock **(the lock circuitry generates a hash of the received input to use for later comparison)** to determine whether or not to grant release of the security function **(column 6, lines 1-67, comparison means of the lock circuitry)**; and
- a memory cell array data output switching circuit for, when an output signal from the determination circuit indicates a matching result of comparison between the value which is generated based on the security release key and the value which is generated based on the security registration lock, permitting data which is read from a corresponding one of the at least one memory cell array block to be externally output **(column 6, lines 1-36, gating circuit receives enabling signal)**.

Regarding claim 2, Vicard teaches the semiconductor storage device further comprises at least one register for retaining an output signal output from the determination circuit (column 5, lines 1-67); and when an output signal output from the at least one register indicates that release of the security function is to be granted, the memory cell array data output switching circuit permits data which is read from a

corresponding one of the at least one memory cell array block to be externally output (column 6, lines 1-67).

Regarding claim 3, Vicard teaches instruction interpretation means for interpreting an externally-input setting instruction to write at least one of the security release key and the security registration lock into the at least one memory region or the at least one non-volatile storage means, respectively (column 6, lines 1-67).

Regarding claim 4, Vicard teaches wherein the determination circuit compares the value which is generated based on the security release key against the value which is generated based on the security registration lock for each of the at least one memory cell array block, and results of comparison are collaterally written in the at least one register (column 5, lines 1-67, column 6, lines 1-67).

Regarding claim 5, Vicard teaches a unidirectional conversion circuit or an encryption circuit, wherein results of converting the security release key and the security registration lock by means of the unidirectional conversion circuit or the encryption circuit are written to the at least one memory region and the at least one non-volatile storage means, respectively (figures 1-3b, column 4, lines 20-67, column 5, lines 1-67).

Regarding claim 6, Vicard teaches which lacks means for reading the security release key and the security registration lock (column 6, lines 45-67, column 7, lines 1-8).

Regarding claim 7, Vicard teaches the at least one non-volatile storage means is a one-time programmable Read Only Memory which prohibits rewriting and erasure;

and rewriting and erasure are prohibited after the security registration lock is written (column 5, lines 1-67, column 6, lines 1-36).

Regarding claim 8, Vicard teaches the at least one non-volatile storage means is a one-time programmable Read Only Memory which prohibits rewriting and erasure; and the semiconductor storage device has a non-volatile lock function for locking the semiconductor storage device to prohibit rewriting and erasure after writing of the security registration lock has been performed (column 5, lines 1-67, column 6, lines 1-36).

Regarding claim 9, Vicard teaches a flag indicating that the security release key has been set, wherein the flag is set automatically or manually after the security release key is written, thereby prohibiting additional writing to the corresponding one of the at least one memory cell array block (column 5, lines 25-67).

Regarding claim 10, Vicard teaches wherein a wait operation is performed while writing the security release key to the at least one memory region (column 6, lines 7-36).

NEW GROUND(S) OF REJECTION

Claim Rejections - 35 USC § 103

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claims 1-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vicard, and further in view of Chuang et al. (US Patent 6,031,757, hereinafter Chuang).

Regarding claim 1, Vicard teaches

- at least one non-volatile memory cell array block which is capable of receiving concurrent electrical erasure **(column 2, lines 30-67, column 5, lines 49-67, functional block)**;
- a key means comprising a security release key **(column 4, lines 20-67, col. 5, lines 25-40, chip-key signature)**;
- a lock means comprising a security registration lock corresponding to each of the at least one memory cell array block **(column 4, lines 20-67, lock circuitry)**;
- at least one memory region, each one of said at least one memory region being provided in the at least one memory cell array block, for storing the security release key **(column 5, lines 1-48, signature stored, col. 5, lines 48-67, signatures H(k1)-H(K6) associated w/ particular blocks)**;
- a determination circuit for comparing a value which is generated based on the security release key **(a signature of the key)** against a value which is generated based on the security registration lock **(the lock circuitry generates a hash of the received input to use for later comparison)** to determine whether or not to grant release of the security function **(column 6, lines 1-67, comparison means of the lock circuitry)**; and
- a memory cell array data output switching circuit for, when an output signal from the determination circuit indicates a matching result of

comparison between the value which is generated based on the security release key and the value which is generated based on the security registration lock, permitting data which is read from a corresponding one of the at least one memory cell array block to be externally output **(column 6, lines 1-36, gating circuit receives enabling signal)**.

Vicard allegedly does not expressly disclose at least one non-volatile storage means for storing the security registration lock.

However, Vicard suggests using secure communications link (abstract) and providing storage means and using Flash and EEPROM memory (col. 5) and Chuang teaches using at least one non-volatile storage means for storing the security registration lock **(abstract, sector lock memory that stores sector lock signals)**.

Therefore, it would have been obvious to someone of ordinary skill in the art at the time the invention was made to use some of this memory or to add more memory to store a particular value to help determine whether to enable access to a functional block and to combine the teachings of Chuang with the system of Vicard.

One of ordinary skill in the art would have been motivated to perform such a modification to use the lock circuitry as a building block to create more complex structures **(Vicard, col.6, lines 30-67, col. 7, lines 1-7, fig. 3, using more chips, automating the key input for a same key)** and to provide write-protect features to specific memory cell arrays **(Chuang, col. 4, lines 15-45)**.

Regarding claim 2, the combination of Vicard with Chuang teaches the semiconductor storage device further comprises at least one register for retaining an

output signal output from the determination circuit (Vicard, column 5, lines 1-67); and when an output signal output from the at least one register indicates that release of the security function is to be granted, the memory cell array data output switching circuit permits data which is read from a corresponding one of the at least one memory cell array block to be externally output (Vicard, column 6, lines 1-67).

Regarding claim 3, the combination of Vicard with Chuang teaches instruction interpretation means for interpreting an externally-input setting instruction to write at least one of the security release key and the security registration lock into the at least one memory region or the at least one non-volatile storage means, respectively (Vicard, column 6, lines 1-67).

Regarding claim 4, the combination of Vicard with Chuang teaches wherein the determination circuit compares the value which is generated based on the security release key against the value which is generated based on the security registration lock for each of the at least one memory cell array block, and results of comparison are collaterally written in the at least one register (Vicard, column 5, lines 1-67, column 6, lines 1-67).

Regarding claim 5, the combination of Vicard with Chuang teaches a unidirectional conversion circuit or an encryption circuit, wherein results of converting the security release key and the security registration lock by means of the unidirectional conversion circuit or the encryption circuit are written to the at least one memory region and the at least one non-volatile storage means, respectively (Vicard, figures 1-3b, column 4, lines 20-67, column 5, lines 1-67).

Regarding claim 6, the combination of Vicard with Chuang teaches which lacks means for reading the security release key and the security registration lock (Vicard, column 6, lines 45-67, column 7, lines 1-8).

Regarding claim 7, the combination of Vicard with Chuang teaches the at least one non-volatile storage means is a one-time programmable Read Only Memory which prohibits rewriting and erasure; and rewriting and erasure are prohibited after the security registration lock is written (Vicard, column 5, lines 1-67, column 6, lines 1-36).

Regarding claim 8, the combination of Vicard with Chuang teaches the at least one non-volatile storage means is a one-time programmable Read Only Memory which prohibits rewriting and erasure; and the semiconductor storage device has a non-volatile lock function for locking the semiconductor storage device to prohibit rewriting and erasure after writing of the security registration lock has been performed (Vicard, column 5, lines 1-67, column 6, lines 1-36).

Regarding claim 9, the combination of Vicard with Chuang teaches a flag indicating that the security release key has been set, wherein the flag is set automatically or manually after the security release key is written, thereby prohibiting additional writing to the corresponding one of the at least one memory cell array block (Vicard, column 5, lines 25-67).

Regarding claim 10, the combination of Vicard with Chuang teaches wherein a wait operation is performed while writing the security release key to the at least one memory region (Vicard, column 6, lines 7-36).

(10) Response to Argument

A.

Regarding Appellant's argument that Vicard does not store a key and a lock, Examiner respectfully points out that Vicard stores multiple values and functions, i.e. Vicard stores a key, claimed "security release key" mapped to Vicard's signature of a key that upon comparison to an entered value, enables unlocking functionality of a memory block, furthermore, Vicard stores a lock circuitry which provides the functionality assigned to the security registration lock. Therefore, the issue becomes an issue of how the elements are labeled, not of what functionality they provide.

Contrary to Appellant's argument that Vicard does not store IV1 and IV2, Examiner submits that Vicard does in fact temporarily stores the values of IV1 and IV2 (col. 4, lines 55-67, temporarily outputs IV1 to the hash function, then the hash function outputs IV2 and uses it to compare against the stored hash values, and col. 5, lines 10-25, the comparison block latches the enable signal).

B.

Regarding Appellant's argument that comparing two keys is not equivalent to comparing a key and a lock, Examiner respectfully submits that the claims are given the broadest reasonable interpretation consistent with the specification, therefore absent some claim language differentiating and defining what a lock is (is it some value stored a priory related to what the block is, i.e. address space), based on the usage afforded by the lock, it reads on Vicard's lock circuitry. The lock only serves a purpose of

comparing to a stored value to allow access to a certain block after a successful comparison is made.

Contrary to Appellant's argument, what is claimed is not that a function is released when a match exists between a received key and a stored lock, but when a match exists between a value generated based on the stored release key and a value generated based on the security registration lock. According to the interpretation of Vicard, then, a match exists between the release key (without an explicit transformation) and a value generated based on the security registration lock (IV2 generated by the lock circuitry, Vicard, col. 5, lines 10-25).

C.

Regarding Appellant's argument that Examiner failed to address certain argument, Examiner respectfully notes that the argument has been that Vicard's signature of a chip-key stored maps to Appellant's security release key and that was the intended response to said argument.

Regarding Appellant's argument that Vicard does not disclose or suggest that the key is stored in the semiconductor storage device, Examiner respectfully submits that Vicard teaches storing the hash in memory (col. 5, lines 25-40).

NEW GROUND(S) OF REJECTION

Chuang has been introduced to support the argument of using additional memory elements to store additional information and teach the argued, but not clearly claimed feature of "at least one non-volatile storage means for storing the security registration lock". Chuang stores sector lock signals for at least one sector in the memory cell array (col. 6, lines 60-67, col. 7, lines 1-15, sector lock bit store).

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

This examiner's answer contains a new ground of rejection set forth in section **(9)** above. Accordingly, appellant must within **TWO MONTHS** from the date of this answer exercise one of the following two options to avoid *sua sponte* **dismissal of the appeal** as to the claims subject to the new ground of rejection:

(1) **Reopen prosecution.** Request that prosecution be reopened before the primary examiner by filing a reply under 37 CFR 1.111 with or without amendment, affidavit or other evidence. Any amendment, affidavit or other evidence must be relevant to the new grounds of rejection. A request that complies with 37 CFR 41.39(b)(1) will be entered and considered. Any request that prosecution be reopened will be treated as a request to withdraw the appeal.

(2) **Maintain appeal.** Request that the appeal be maintained by filing a reply brief as set forth in 37 CFR 41.41. Such a reply brief must address each new ground of rejection as set forth in 37 CFR 41.37(c)(1)(vii) and should be in compliance with the other requirements of 37 CFR 41.37(c). If a reply brief filed pursuant to 37 CFR 41.39(b)(2) is accompanied by any amendment, affidavit or other evidence, it shall be treated as a request that prosecution be reopened before the primary examiner under 37 CFR 41.39(b)(1).

Extensions of time under 37 CFR 1.136(a) are not applicable to the TWO MONTH time period set forth above. See 37 CFR 1.136(b) for extensions of time to reply for patent applications and 37 CFR 1.550(c) for extensions of time to reply for ex parte reexamination proceedings.

Respectfully submitted,

/David García Cervetti/

A Technology Center Director or designee must personally approve the new ground(s) of rejection set forth in section (9) above by signing below:

KIM VU
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

Conferees:

Kim Y. Vu

SPE

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